IN THE UNITED STATES PATENT & TRADEMARK OFFICE

Applicant:	Kao et al.	Docket No:	16405-0311
Serial No:	09/256,265	Group Art Unit	2815
Filing Date:	February 23, 1999	Examiner:	Diaz, J.

Title: "METHOD AND APPARATUS FOR SPLIT GATE SOURCE SIDE INJECTION FLASH MEMORY CELL AND ARRAY WITH DEDICATED ERASE GATES"

Box Fee Amendment
Assistant Commissioner for Patents
Washington, D.C. 20231

AMENDMENT

Examiner:

Responsive to the Office Action mailed on October 3, 2000, please amend the Application as follows and consider the following remarks:

In the Claims:

Cancel claims 3-7 and 11-15 without prejudice:

1. (Once Amended) A semiconductor device having at least one transistor, the device comprising:

a substrate having a channel region defined thereon;

[a defined channel region;]

a first insulating layer disposed over said channel region and over at least a portion of said substrate;

a floating gate generally disposed over said channel region and separated therefrom by [a] said first insulating layer, said floating gate having at least two side walls and a top surface;

a second insulating layer disposed over said side walls and over said top surface of said floating gate;

a control gate [generally placed on one side] formed over a first one of said side walls and over at least a portion of said top surface of said floating gate and being separated from said